AGILENT TECHNOLOGIES, INC.
Legal Department, DL429
Intellectual Property Administration
P. O. Box 7599
Loveland, Colorado 80537-0599

ATTORNEY DOCKET NO. 10010863-1

APS

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Louise A. Koss et al.

Serial No.: 10/008,382 **Examiner:** James C. Kerveros

Filing Date: December 5, 2001 **Group Art Unit:** 2133

Title: Apparatus for Random Access Memory Array Self-Test

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Sir:

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on June 8, 2005 .

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) **$500.00**.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

☐ (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)(1)-(5)) for the total number of months checked below:

☐	one month	$ 120.00
☐	two months	$ 450.00
☐	three months	$1020.00
☐	four months	$1590.00

☐ The extension fee has already been filled in this application.

☒ (b) Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account **50-1078** the sum of $500.00 . At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account **50-1078** pursuant to 37 CFR 1.25.

A duplicate copy of this transmittal letter is enclosed.

Respectfully submitted,

Louise A. Koss et al.

By Morley C. Tobey, Jr.

Morley C. Tobey, Jr.
Attorney/Agent for Applicant(s)

Reg. No. 43,955

Date: July 22, 2005

Telephone No. (970) 669-1266

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AGILENT TECHNOLOGIES, INC.
Legal Department, DL429
Intellectual Property Administration
P.O. Box 7599
Loveland, Colorado 80537-0599

PATENT APPLICATION
ATTORNEY DOCKET NO. 10010863-1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: **Louise A. Koss et al.**	Confirmation Number: **2960**
Serial No.: **10/008,382**	Examiner: **James C. Kerveros**
Filed: **December 5, 2001**	Group Art Unit: **2133**
For: **Apparatus for Random Access Memory Self-Test**	

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

INTRODUCTION

Pursuant to the provisions of 37 C.F.R §1.191 *et seq.*, Applicant hereby appeals to the Board of Patent Appeals and Interferences (the "Board") from the examiner's final rejection dated 02/08/2005. A Response After Final Office Action under 37 CFR §1.116 was timely filed by Applicant on 04/18/2005. Subsequently Examiner

issued an Advisory Action on 05/16/2005. A Notice of Appeal was timely filed on 06/08/2005, in accordance with 37 CFR §1.8. This brief on appeal is accompanied by the requisite fee (37 C.F.R §1.192(a) and §1.17(c)).

REAL PARTY IN INTEREST

The entire interest in the present application has been assigned to Agilent Technologies, Inc. as recorded at Reel 012862, Frame 0711 on 04/29/2002.

RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

STATUS OF CLAIMS

Claims 1-8 are pending.

Claims 1-8 have been finally rejected.

Claims 1-8 are on appeal.

STATUS OF AMENDMENTS

An Amendment/Response After Final Office Action under 37 CFR §1.116 was filed by Applicant on 04/18/2005. That Amendment was denied entry into the Application per the Advisory Action on 05/16/2005. However, the only change in the Amendment of 04/18/2005 was to cancel claim 9 which appears to have been

accepted per the Advisory Action on 05/16/2005. There are no outstanding amendments.

SUMMARY OF CLAIMED SUBJECT MATTER

The summary is set forth in several exemplary embodiments that correspond to the independent claims. Discussions about elements and recitations of these claims can be found at least at the cited locations in the specification and drawings.

CLAIM 1: (Independent)

Claim 1 claims an electronic circuit (**[200]** on page 6, lines 23-24 and Figure 2 for example) for self-test of a random access memory array (**[250]** on page 5, lines 25-28 and Figure 1 for example). The random access memory array has a plurality of memory storage cells (**[110]** on page 6, lines 25-28 and Figure 2 for example) in a RAM circuit (**[105]** on page 5, lines 20-21 and Figure 1 for example). The storage cells are organized into a plurality of slice arrays (**[118]** on page 6, lines 11-13 and Figure 1 for example). The slice arrays comprise a control circuit (**[210]** on page 6, lines 15-16 and Figure 2 for example), an address selection circuit (**[120]** on page 6, lines 15-16 and Figure 2 for example), one input/output circuit (**[130]** on page 6, lines 14-15 and Figure 2 for example) each associated with each slice array (Figure 2 for example), and an error detection circuit (**[230]** on page 6, lines 18-20 and Figure 2 for example). The control circuit is embedded in a control and address block of the RAM circuit (claim 3 as originally filed and Figure 3 for example). The control circuit directs the address selection circuit to index through memory addresses (page 3, lines 7-8 and Figure 3 for example). The control circuit directs each input/output circuit to write data into its associated slice array at an indexed memory address (page 3, lines 9-10 and Figure 2 for example), to read data from the associated slice array at the indexed memory address (page 3, lines 9-11 and Figure 2 for example), and to

compare the data read from the associated slice array with that written into the associated slice array at the indexed memory address (page 3, lines 11-12 and Figure 2 for example). The error detection circuit collects results of self-test data comparisons from each input/output circuit (page 3, lines 12-14 and Figure 2 for example) and notifies the control circuit of the results of the self-test data comparisons (page 3, lines 12-14 and Figure 2 for example).

CLAIM 2: (Dependent)

Claim 2 claims the electronic circuit (**[200]** on page 6, lines 23-24 and Figure 2 for example) as recited in claim 1. In claim 2, the electronic circuit is embedded within the RAM circuit (claim 2 as originally filed and Figure 2 for example) in an integrated circuit (claim 2 as originally filed for example).

CLAIM 3: (Dependent)

Claim 3 claims the electronic circuit (**[200]** on page 6, lines 23-24 and Figure 2 for example) as recited in claim 1. In claim 3, the address selection circuit is embedded in the control and address block of the RAM circuit (claim 3 as originally filed and Figure 2 for example).

CLAIM 7: (Dependent)

Claim 7 claims the electronic circuit (**[200]** on page 6, lines 23-24 and Figure 2 for example) as recited in claim 1. In claim 7, the input/output circuit comprises a data-in multiplexer (**[1305]** on page 10, lines 13-16 and Figure 3 for example), an input register (**[381]** on page 10, lines 13-16 and Figure 3 for example), an inverter (**[1315]** on page 10, lines 13-16 and Figure 3 for example), an input-complement multiplexer (**[1320]** on page 10, lines 13-16 and Figure 3 for example), an output-complement multiplexer (**[1330]** on page 10, lines 13-16 and Figure 3 for example), an output register (**[383]** on page 10, lines 13-16 and Figure 3 for example), and an exclusive-OR gate (**[1340]** on page 10, lines 13-16 and Figure 3 for example). The data-in multiplexer has first and second data-in-multiplexer inputs (**[1306,1307]** on

page 10, lines 22-23 and Figure 3 for example) and a data-in-multiplexer output (**[1309]** on page 10, lines 22-23 and Figure 3 for example). The first data-in-multiplexer input is configured to receive the self-test data (page 10, lines 24-25 and Figure 3 for example). The second data-in-multiplexer input is configured to receive normal operational data (page 10, lines 24-25 and Figure 3 for example). When the data-in multiplexer receives command from the control circuit to perform the self-test, the value of the first data-in-multiplexer input is transferred to the data-in-multiplexer output (page 10, lines 26-30 and Figure 3 for example). Otherwise, the second data-in-multiplexer input is configured to transfer its value to the data-in-multiplexer output (page 10, line 30 through page 11, line 5 and Figure 3 for example). The output of the data-in-multiplexer output is connected to the input of the input register (page 11, lines 6-7 and Figure 3 for example). The output of the input register is connected to the input of the inverter (**[1315]** on page 11, lines 6-7 and Figure 3 for example). The input-complement multiplexer has first and second input-complement-multiplexer inputs (**[1321,1322]** on page 11, lines 8-10 and Figure 3 for example) and an input-complement-multiplexer output (**[1324]** on page 11, lines 8-10 and Figure 3 for example). The output of the input register is connected to the first input-complement-multiplexer input (page 11, lines 10-11 and Figure 3 for example). The output of the inverter is connected to the second input-complement-multiplexer input (on page 11, lines 11-12 and Figure 3 for example). When, the control circuit instructs the input-complement multiplexer to write test data into the slice array, the value of the first input-complement-multiplexer input is transferred to the input-complement-multiplexer output (page 11, lines 19-24 and Figure 3 for example). Otherwise, the value of the second input-complement-multiplexer input is transferred to the input-complement-multiplexer output (page 11, lines 24-29 and Figure 3 for example). The output-complement multiplexer has first and second output-complement-multiplexer inputs (**[1331,1332]** on page 11, lines 13-15 and Figure 3 for example) and an output-complement-multiplexer output (**[1334]** on page 11, lines 13-15 and Figure 3 for example). The output of the input register is connected to the first output-complement-multiplexer input (page 11, lines 15-18 and Figure 3 for

example). The output of the inverter is connected to the second output-complement-multiplexer input (page 11, lines 11-12 and Figure 3 for example). When the control circuit instructs the output-complement multiplexer to compare test data to data in the slice array, the value of the first output-complement-multiplexer input is transferred to the output-complement-multiplexer output (page 12, lines 13-18 and Figure 3 for example). Otherwise, the value of the second output-complement-multiplexer input is transferred to the output-complement-multiplexer output (page 12, lines 18-22 and Figure 3 for example). The output register receives the contents of the slice array (page 10, lines 11-12 and Figure 3 for example). The exclusive-OR gate has first and second exclusive-OR-gate inputs (**[1341,1342]** on page 12, lines 27-28 and Figure 3 for example) and an exclusive-OR-gate output (**[1343]** on page 12, lines 27-28 and Figure x for example). The output of the output register is connected to the first exclusive-OR-gate input (page 12, lines 28-29 and Figure 3 for example). The output-complement-multiplexer output is connected to the second exclusive-OR-gate input (page 12, lines 29-30 and Figure 3 for example).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The grounds of rejection to be reviewed on appeal are as follows:

(1) Claims 1-6, 8, and 9 were rejected under 35 U.S.C. § 102(e) as being anticipated by Bhavsar et al. in U.S. Patent Number 6,408,401 entitled "Embedded RAM with Self-Test and Self-Repair with Spare Rows and Columns" hereinafter *Bhavsar*.

(2) Claim 7 was rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over *Bhavsar* in view of Gupta et al. in U.S. Patent Number 6,609,222 entitled "Methods and Circuitry for Built-In Self-Testing of Content Addressable Memories" hereinafter *Gupta*.

ARGUMENT

1. REJECTION OF CLAIMS 1-6, & 8 UNDER U.S.C. § 102(e): [*Bhavsar*]

In the first paragraph on page 3 of the Final Office Action having DATE MAILED of 8 February 2005 (Paper No./Mail Date 20050202) referred to hereinafter as the Final Office Action of 8 February 2005, claims 1-6 and 8 were rejected under 35 U.S.C. § 102(e) as being anticipated by Bhavsar et al. in U.S. Patent Number 6,408,401 entitled "Embedded RAM with Self-Test and Self-Repair with Spare Rows and Columns" hereinafter *Bhavsar*. Applicant respectively traverses.

As stated in MPEP 2131 "To anticipate a claim, the reference must teach every element of the claim." As will be shown in the following paragraphs, *Bhavsar* fails to teach every element of claims 1-6 and 8.

1.1 Claim 1 & 4-6:

Among other items, *Bhavsar* does not disclose a control circuit "embedded in a control and address block of a RAM circuit" which is an element of claim 1 of the Present Application. *Bhavsar* discloses "Logic **201** for performing a self-test and self-repair algorithm also resides on the chip **12**, and communicates with the RAM **80** via the memory bus **20**" (*Bhavsar*: column 4, lines 14-16), but does not disclose a control circuit "embedded in a control and address block of a RAM circuit" as in claim 1. Figure 1 of *Bhavsar* shows logic **201** remotely located from RAM cache **80** and communicating with RAM cache **80** via memory bus **20** but does NOT show logic **201** embedded in the RAM cache **80**.

On page 8 the Final Office Action of 8 February 2005 argues that the RAM Test Algorithm Engine **207** of *Bhavsar* (alleged to be analogous to the control circuit of the Present Application) is embedded because it is integrated in the logic circuit **201** and "by virtue that the target RAM segment **251** is also embedded on chip **12**". The Final Office Action of 8 February 2005 states that a definition of the word "embedded" is "to make integral part of". Applicant notes that a definition of the word "in" is "within the limits, bounds, or area of " and that the phrase "embedded in"

is used in claim 1. Using these definitions, claim 1 implies that the control circuit is an integral part of and within the limits of a control and address block of the RAM circuit. While both the RAM Test Algorithm Engine **207** and the RAM segment **251** of *Bhavsar* may be embedded in chip **12**, the RAM Test Algorithm Engine **207** is NOT embedded in the RAM segment **251**.

Thus, Applicant has demonstrated that *Bhavsar* fails to teach every element of claim 1. Because *Bhavsar* fails to teach every element of claim 1 as required by MPEP 2131, *Bhavsar* does not anticipate claim 1. In addition, *Bhavsar* fails to suggest every element of claim 1. Thus, claim 1 is allowable over *Bhavsar*.

Because dependent claims 4-6 depend from independent claim 1, it is noted that dependent claims 4-6 have all the features described above for claim 1 as elements. As demonstrated above, independent claim 1 is not anticipated by *Bhavsar*, nor does *Bhavsar* suggest every element of claim 1. For this and other reasons, claims 4-6 differ from *Bhavsar*.

Thus, Applicant has demonstrated that *Bhavsar* fails to teach every element of claims 4-8. Because *Bhavsar* fails to teach every element of claims 4-6 as required by MPEP 2131, *Bhavsar* does not anticipate claims 4-6. In addition, *Bhavsar* fails to suggest every element of claims 4-6. Thus, claims 4-6 are allowable over *Bhavsar*.

1.2 Claim 2:

In the third paragraph on page 4, Final Office Action of 8 February 2005 alleges that "*Bhavsar* discloses an electronic circuit **201** embedded in a RAM circuit chip **12** in an integrated circuit." However as shown above, *Bhavsar*, among other items, does NOT disclose an electronic circuit analogous to that of the Present Application "embedded within the RAM circuit" as is claimed in claim 2 of the Present Application. In *Bhavsar* "each chip **12** comprises some core logic **16**, which may contain, for example, arithmetic or floating point logic units and registers. In addition, each chip comprises an on-chip RAM cache **80**." (*Bhavsar*: column 4, lines 5-8). *Bhavsar* does NOT disclose an electronic circuit analogous to that of the Present Application in the RAM cache **80**.

In addition, because dependent claim 2 depends from independent claim 1, it is noted that dependent claim 2 has all the features described above for claim 1 as elements. As demonstrated above, independent claim 1 is not anticipated by *Bhavsar*, nor does *Bhavsar* suggest every element of claim 1.

Among other items in claim 1, *Bhavsar* does not disclose a control circuit "embedded in a control and address block of a RAM circuit" which is an element of claim 1 of the Present Application. *Bhavsar* discloses "Logic **201** for performing a self-test and self-repair algorithm also resides on the chip **12**, and communicates with the RAM **80** via the memory bus **20**" (*Bhavsar*: column 4, lines 14-16), but does not disclose a control circuit "embedded in a control and address block of a RAM circuit" as in claim 1. Figure 1 of *Bhavsar* shows logic **201** remotely located from RAM cache **80** and communicating with RAM cache **80** via memory bus **20** but does NOT show logic **201** embedded in the RAM cache **80**.

On page 8 the Final Office Action of 8 February 2005 argues that the RAM Test Algorithm Engine **207** of *Bhavsar* (alleged to be analogous to the control circuit of the Present Application) is embedded because it is integrated in the logic circuit **201** and "by virtue that the target RAM segment **251** is also embedded on chip **12**". The Final Office Action of 8 February 2005 states that a definition of the word "embedded" is "to make integral part of". Applicant notes that a definition of the word "in" is "within the limits, bounds, or area of " and that the phrase "embedded in" is used in claim 1. Using these definitions, claim 1 implies that the control circuit is an integral part of and within the limits of a control and address block of the RAM circuit. While both the RAM Test Algorithm Engine **207** and the RAM segment **251** of *Bhavsar* may be embedded in chip **12**, the RAM Test Algorithm Engine **207** is NOT embedded in the RAM segment **251**.

Thus, Applicant has demonstrated that *Bhavsar* fails to teach every element of claim 2. Because *Bhavsar* fails to teach every element of claim 2 as required by MPEP 2131, *Bhavsar* does not anticipate claim 2. In addition, *Bhavsar* fails to suggest every element of claim 2. Thus, claim 2 is allowable over *Bhavsar*.

1.3 Claim 3:

In the fourth paragraph on page 4, the Final Office Action of 8 February 2005 alleges that "*Bhavsar* discloses a control circuit (RAM Test Algorithm Engine **207**) and address selection circuit (Address and Read/Write Data path logic **255**), which are embedded in a control and address block of the RAM circuit chip **12**." Applicant notes that The Final Office Action of 8 February 2005 failed to identify which element disclosed in *Bhavsar* was considered to be analogous to the control and address block of the RAM circuit of claim 3 of the Present Application. As such it is difficult, if not impossible, for Applicant to fully address this rejection. However, Applicant notes that in Figure 2 the RAM Test Algorithm Engine **207** is included in logic **201**, whereas the Address and Read/Write Data Path Logic **255** is a part of the RAM segment **251**. The only common container within which the RAM Test Algorithm Engine **207** and the Address and Read/Write Data path logic **255** reside appears to be the chip **12** NOT a control and address block of the RAM circuit. Thus, in addition to other items, claim 3 differs from *Bhavsar* as indicated above.

In addition, because dependent claim 3 depends from independent claim 1, it is noted that dependent claim 3 has all the features described above for claim 1 as elements. As demonstrated above, independent claim 1 is not anticipated by *Bhavsar*, nor does *Bhavsar* suggest every element of claim 1. For this and other reasons, claim 3 differs from *Bhavsar*.

Among other items in claim 1, *Bhavsar* does not disclose a control circuit "embedded in a control and address block of a RAM circuit" which is an element of claim 1 of the Present Application. *Bhavsar* discloses "Logic **201** for performing a self-test and self-repair algorithm also resides on the chip **12**, and communicates with the RAM **80** via the memory bus **20**" (*Bhavsar*: column 4, lines 14-16), but does not disclose a control circuit "embedded in a control and address block of a RAM circuit" as in claim 1. Figure 1 of *Bhavsar* shows logic **201** remotely located from RAM cache **80** and communicating with RAM cache **80** via memory bus **20** but does NOT show logic **201** embedded in the RAM cache **80**.

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Thus, Applicant has demonstrated that *Bhavsar* fails to teach every element of claim 3. Because *Bhavsar* fails to teach every element of claim 3 as required by MPEP 2131, *Bhavsar* does not anticipate claim 3. In addition, *Bhavsar* fails to suggest every element of claim 3. Thus, claim 3 is allowable over *Bhavsar*.

1.4 Claim 8:

The Final Office Action of 8 February 2005 rejected dependent claim 8 under 35 U.S.C. § 102(e) but did not reject claim 7 upon which claim 8 depends. Because dependent claim 8 depends from dependent claim 7, it is noted that dependent claim 8 has all the features described above for claim 7 as elements. Since claim 7 has not been rejected as being anticipated by *Bhavsar*, claim 8 comprises elements which The Final Office Action of 8 February 2005 did not identify as being taught by *Bhavsar*. Thus, *Bhavsar* does not anticipate, nor does *Bhavsar* suggest every element of claim 8.

In addition, because dependent claim 8 depends from independent claim 1 via dependent claim 7, it is noted that dependent claim 8 has all the features described above for claim 1 as elements. As demonstrated above, independent claim 1 is not

anticipated by *Bhavsar*, nor does *Bhavsar* suggest every element of claim 1. For this and other reasons, claim 8 differs from *Bhavsar*.

Thus, Applicant has demonstrated that *Bhavsar* fails to teach every element of claim 8. Because *Bhavsar* fails to teach every element of claim 8 as required by MPEP 2131, *Bhavsar* does not anticipate claim 8. In addition, *Bhavsar* fails to suggest every element of claim 8. Thus, claim 8 is allowable over *Bhavsar*.

2. REJECTION OF CLAIM 7 UNDER 35 U.S.C. § 103(a): [*Bhavsar & Gupta*]

In the second paragraph on page 6 of The Final Office Action of 8 February 2005, claim 7 was rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over *Bhavsar* in view of Gupta et al. in U.S. Patent Number 6,609,222 entitled "Methods and Circuitry for Built-In Self-Testing of Content Addressable Memories" hereinafter *Gupta*. Applicant respectfully traverses.

> Referring to MPEP 2142, "To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations."

2.1 Claim 7:

With respect to the rejection of claim 7 under 35 U.S.C. § 103(a), the Final Office Action of Action of 8 February 2005 points out the following multiplexers: (1) multiplexers (322) & (324) used for addressing the memory of *Gupta*, (2) multiplexer (326) used for writing BIST or functional data, and (3) multiplexer (320) which accepts search data from a BIST search interface and functional data for an

operational search. However, neither *Bhavsar* nor *Gupta* disclose the following elements & combination of elements: (1) "an input register, wherein the output of the data-in-multiplexer output is connected to the input of the input register", (2) "an inverter, wherein the output of the input register is connected to the input of the inverter", and (3) "an input-complement multiplexer, wherein the input-complement multiplexer has first and second input-complement-multiplexer inputs and an input-complement-multiplexer output, wherein the output of the input register is connected to the first input-complement-multiplexer input, wherein the output of the inverter is connected to the second input-complement-multiplexer input, and wherein: when, the control circuit instructs the input-complement multiplexer to write test data into the slice array, the value of the first input-complement-multiplexer input is transferred to the input-complement-multiplexer output, otherwise, the value of the second input-complement-multiplexer input is transferred to the input-complement-multiplexer output".

Further, it is noted that dependent claim 7 depends from independent claim 1 and that, as such, dependent claim 7 has all the features described above for claim 1 as elements. Among other items in claim 1, *Bhavsar* does not disclose a control circuit "embedded in a control and address block of a RAM circuit" which is an element of claim 1 of the Present Application. *Bhavsar* discloses "Logic **201** for performing a self-test and self-repair algorithm also resides on the chip **12**, and communicates with the RAM **80** via the memory bus **20**" (*Bhavsar*: column 4, lines 14-16), but does not disclose a control circuit "embedded in a control and address block of a RAM circuit" as in claim 1. Figure 1 of *Bhavsar* shows logic **201** remotely located from RAM cache **80** and communicating with RAM cache **80** via memory bus **20** but does NOT show logic **201** embedded in the RAM cache **80**.

On page 8 the Final Office Action of 8 February 2005 argues that the RAM Test Algorithm Engine **207** of *Bhavsar* (alleged to be analogous to the control circuit of the Present Application) is embedded because it is integrated in the logic circuit **201** and "by virtue that the target RAM segment **251** is also embedded on chip **12**". The Final Office Action of 8 February 2005 states that a definition of the word

"embedded" is "to make integral part of". Applicant notes that a definition of the word "in" is "within the limits, bounds, or area of " and that the phrase "embedded in" is used in claim 1. Using these definitions, claim 1 implies that the control circuit is an integral part of and within the limits of a control and address block of the RAM circuit. While both the RAM Test Algorithm Engine **207** and the RAM segment **251** of *Bhavsar* may be embedded in chip **12**, the RAM Test Algorithm Engine **207** is NOT embedded in the RAM segment **251**.

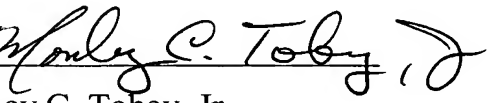
Thus, the cited references do not teach nor do they suggest all the claim limitations of claim 7 as required by MPEP 2142. As such, claim 7 is not obvious over *Bhavsar*, and it follows that claim 7 is allowable.

3. SUMMARY & CONCLUSION:

In summary, the art of record does not teach nor does it suggest all the elements of the pending claims. Thus, the Present Application is nonobvious over the cited art.

Applicant respectfully requests the Board to reverse the final rejection and to order the examiner to pass this application to allowance and issue.

Respectfully submitted,

by 

Morley C. Tobey, Jr.

Reg. No. 43,955

July 22, 2005

Loveland, CO 80537

(970) 669-1266

CLAIM APPENDIX

Claims 1-8 are presented below in their final accepted form as amended under 37 CFR §1.116 following final rejection on 02/08/2005.

1. An electronic circuit for self-test of a random access memory array having a plurality of memory storage cells in a RAM circuit, wherein the storage cells are organized into a plurality of slice arrays, comprising:

a control circuit, wherein the control circuit is embedded in a control and address block of the RAM circuit;

an address selection circuit, wherein the control circuit directs the address selection circuit to index through memory addresses;

one input/output circuit each associated with each slice array, wherein the control circuit directs each input/output circuit to write data into its associated slice array at an indexed memory address, to read data from the associated slice array at the indexed memory address, and to compare the data read from the associated slice array with that written into the associated slice array at the indexed memory address; and

an error detection circuit, wherein the error detection circuit collects results of self-test data comparisons from each input/output circuit and notifies the control circuit of the results of the self-test data comparisons.

2. The electronic circuit as recited in claim 1, wherein the electronic circuit is embedded within the RAM circuit in an integrated circuit.

3. The electronic circuit as recited in claim 1, wherein the address selection circuit is embedded in the control and address block of the RAM circuit.

4. The electronic circuit as recited in claim 1, wherein the control circuit initiates and terminates the self-test at preselected conditions, wherein the address selection circuit, informs the control circuit when the indexed memory address equals an initial self-test memory address, and wherein the address selection circuit, informs the control circuit when the indexed memory address equals a final self-test memory address.

5. The electronic circuit as recited in claim 1, wherein the address selection circuit comprises:

an address multiplexer, wherein the address multiplexer has first, second, and third address-multiplexer inputs and an address-multiplexer output, wherein the second address-multiplexer input receives the memory address at which the self-test is initiated, wherein the third address-multiplexer input is configured to receive normal operational data addresses, and wherein when the address multiplexer receives command from the control circuit to initiate the self-test, the value of the second address-multiplexer input is transferred to the address-multiplexer output;

a register, wherein the address-multiplexer output is connected to the input of the register and wherein the content of the register is used to address the RAM memory in writing and reading self-test data;

a sequencer, wherein the output of the register is connected to the input of the sequencer, wherein the sequencer outputs an indexed version of the address received at the input of the sequencer, and wherein the output of the sequencer is connected to the first address-multiplexer input; and

a comparator, wherein the output of the register is connected to the input of the comparator, wherein the comparator has first and second comparator outputs, wherein comparator first and second outputs are connected to the control circuit, wherein the first comparator output indicates when the register contains an initial self-test memory address, and wherein the second comparator output indicates when the register contains a final self-test memory address.

6. The electronic circuit as recited in claim 5, wherein the address multiplexer, the register, the sequencer, and the comparator are embedded in a control and address block of the RAM circuit.

7. The electronic circuit as recited in claim 1, wherein the input/output circuit comprises:

a data-in multiplexer, wherein the data-in multiplexer has first and second data-in-multiplexer inputs and a data-in-multiplexer output, wherein the first data-in-multiplexer input is configured to receive the self-test data, wherein the second data-in-multiplexer input is configured to receive normal operational data, and wherein:

when the data-in multiplexer receives command from the control circuit to perform the self-test, the value of the first data-in-multiplexer input is transferred to the data-in-multiplexer output,

otherwise, the second data-in-multiplexer input is configured to transfer its value to the data-in-multiplexer output;

an input register, wherein the output of the data-in-multiplexer output is connected to the input of the input register;

an inverter, wherein the output of the input register is connected to the input of the inverter;

an input-complement multiplexer, wherein the input-complement multiplexer has first and second input-complement-multiplexer inputs and an input-complement-multiplexer output, wherein the output of the input register is connected to the first input-complement-multiplexer input, wherein the output of the inverter is connected to the second input-complement-multiplexer input, and wherein:

when, the control circuit instructs the input-complement multiplexer to write test data into the slice array, the value of the first input-complement-multiplexer input is transferred to the input-complement-multiplexer output,

otherwise, the value of the second input-complement-multiplexer input is transferred to the input-complement-multiplexer output;

an output-complement multiplexer, wherein the output-complement multiplexer has first and second output-complement-multiplexer inputs and an output-complement-multiplexer output, wherein the output of the input register is connected to the first output-complement-multiplexer input, wherein the output of the inverter is connected to the second output-complement-multiplexer input, and wherein:

when, the control circuit instructs the output-complement multiplexer to compare test data to data in the slice array, the value of the first output-complement-multiplexer input is transferred to the output-complement-multiplexer output,

otherwise, the value of the second output-complement-multiplexer input is transferred to the output-complement-multiplexer output;

an output register, wherein the output register receives the contents of the slice array; and

an exclusive-OR gate, wherein the exclusive-OR gate has first and second exclusive-OR-gate inputs and an exclusive-OR-gate output, wherein the output of the output register is connected to the first exclusive-OR-gate input, and wherein the output-

complement-multiplexer output is connected to the second exclusive-OR-gate input.

8. The electronic circuit as recited in claim 7, wherein the input to the error detection circuit is connected to the exclusive-OR-gate output.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.